WHAT IS CLAIMED IS:

1. A programmable circuit operable to:

receive firmware from an external source, the firmware representing a configuration;

store the firmware in a memory; and

download the firmware from the memory.

2. The programmable circuit of claim 1, further operable to operate in the configuration after downloading the firmware from the memory.

3. The programmable circuit of claim 1 wherein the memory comprises a nonvolatile memory.

4. The programmable circuit of claim 1 wherein the memory comprises an external memory.

5. A programmable circuit operable to:

download from a memory first firmware that represents a first configuration;

operate in the first configuration;

download from the memory second firmware that represents a second configuration; and

operate in the second configuration.

6. The programmable circuit of claim 5 wherein the programmable circuit is further operable to:

receive the second firmware from an external source while operating in the first configuration; and

storing the second firmware in the memory while operating in the first configuration.

7. A programmable-circuit unit, comprising:

a memory; and

a programmable circuit coupled to the memory and operable to,

receive firmware from an external source, the firmware representing a configuration of the programmable circuit,

store the firmware in the memory, and

download the firmware from the memory.

8. The programmable-circuit unit of claim 7 wherein the memory comprises an electrically erasable and programmable read-only memory.

9. The programmable-circuit unit of claim 7 wherein the programmable circuit comprises a field-programmable gate array.

10. A programmable-circuit unit, comprising:

a memory operable to store first and second firmware data that respectively represent first and second configurations; and

a programmable circuit coupled to the memory and operable to,

download the first firmware from the memory,

operate in the first configuration,

download the second firmware from the memory, and

operate in the second configuration.

11. The programmable-circuit unit of claim 10 wherein the programmable circuit is further operable to:

receive the second firmware from an external source while operating in the first configuration; and

store the second firmware in the memory while operating in the first configuration.

12. The programmable-circuit unit of claim 10 wherein the programmable circuit is operable to load the second firmware while operating in the first configuration.

13. A programmable-circuit unit, comprising:

a memory operable to store first, second, third, and fourth firmware that respectively represent first, second, third, and fourth configurations;

a first programmable circuit coupled to the memory and operable to,

download the first firmware from the memory,
operate in the first configuration,
download the second firmware from the memory, and
operate in the second configuration; and

a second programmable circuit coupled to the memory and to the first programmable circuit and operable to,

download the third firmware data from the memory,
operate in the third configuration,
download the fourth firmware from the memory, and
operate in the fourth configuration.

14. The programmable-circuit unit of claim 13 wherein the first programmable circuit is further operable to:

receive the second and fourth firmware from an external source while operating in the first configuration; and

store the second and fourth firmware in the memory while operating in the first configuration.

15. The programmable-circuit unit of claim 13 wherein the first and second programmable circuits comprise respective field-programmable gate arrays.

16. A computing machine, comprising:

a processor; and

a programmable-circuit unit coupled to the processor and comprising,

a memory, and

a programmable circuit coupled to the memory and operable to,

receive from the processor firmware that represents a configuration of the programmable circuit,

store the firmware in the memory, and

download the firmware from the memory in response to the processor.

17. The computing machine of claim 16 wherein the processor is operable to:

before sending the firmware to the programmable circuit, determine whether the firmware is already stored in the memory; and

send the firmware to the programmable circuit only if the firmware is not already stored in the memory.

18. The computing machine of claim 16, further comprising:

a configuration registry coupled to the processor and operable to store the firmware and to indicate that the firmware represents a desired configuration for the programmable circuit; and

wherein the processor is operable to download the firmware from the configuration registry to the programmable circuit.

19. The computing machine of claim 16, wherein:

the programmable-circuit unit comprises a pipeline unit; and

the programmable circuit includes a hardwired pipeline that is operable to operate on data.

20. A computing machine, comprising:

a processor; and

programmable-circuit unit coupled to the processor and comprising,

a memory operable to store first and second firmware that respectively represent first and second configurations; and

a programmable circuit operable to,

download the first firmware from the memory,

operate in the first configuration,

download the second firmware from the memory in response to the processor, and

operate in the second configuration.

21. The computing machine of claim 20 wherein:

the processor comprises a first test port;

the programmable-circuit unit comprise a second test port that is coupled to the first test port; and

the processor is operable to load the first firmware into memory via the first and second test ports.

22. The computing machine of claim 20 wherein:

the processor comprises a first test port;

the programmable-circuit unit comprise a second test port that is coupled to the first test port;

while operating in the first configuration, the programmable circuit is operable to perform a self test and to provide self-test data to the processor via the first and second test ports; and

the processor is operable to cause the programmable circuit to download the second firmware from memory only if the self-test data indicates a predetermined result of the self test.

23. The computing machine of claim 20 wherein:

the processor is operable to send the second firmware to the programmable circuit; and

while operating in the first configuration, the programmable circuit is operable to load the second firmware into the memory in response to the processor.

24. A computing machine, comprising:

a processor; and

programmable-circuit unit coupled to the processor and comprising,

a memory operable to store first, second, third, and fourth firmware that respectively represent first, second, third, and fourth configurations,

a first programmable circuit coupled to the memory and operable to,

download the first firmware from the memory,

operate in the first configuration,

download the second firmware from the memory in response to the processor, and

operate in the second configuration, and

a second programmable circuit coupled to the memory and to the first programmable circuit and operable to,

download the third firmware from the memory,

operate in the third configuration,

download the fourth firmware from the memory in response to the processor, and

operate in the fourth configuration.

25. The computing machine of claim 24 wherein:

the processor comprises a first test port;

the programmable-circuit unit comprise a second test port that is coupled to the first test port; and

the processor is operable to load the first and third firmware into memory via the first and second test ports.

26. The computing machine of claim 24 wherein:

the processor comprises a first test port;

the programmable-circuit unit comprise a second test port that is coupled to the first test port;

while operating in the first configuration, the first programmable circuit is operable to perform a first self test and to provide first self-test data to the processor via the first and second test ports;

while operating in the third configuration, the second programmable circuit is operable to perform a second self test and to provide second self-test data to the processor via the first and second test ports; and

the processor is operable to cause the first and second programmable circuits to respectively load the second and fourth firmware from the memory only if the first and second self-test data indicate respective predetermined results of the first and second self tests.

27. The computing machine of claim 24 wherein:

the processor is operable to send the second and fourth firmware to the first programmable circuit; and

while operating in the first configuration, the first programmable circuit is operable to load the second and fourth firmware into the memory in response to the processor.

28. The computing machine of claim 24 wherein the memory comprises:

a first memory section coupled to the first programmable circuit and operable to store the first and second firmware; and

a second memory section coupled to the first and second programmable circuits and operable to store the third and fourth firmware.

29. The computing machine of claim 28 wherein the first and second memory sections are respectively disposed on first and second integrated circuits.

30. A method, comprising:

providing firmware to a programmable circuit, the firmware representing a configuration of the circuit;

storing the configuration data in a memory with the programmable circuit; and

downloading the configuration data from the memory into the programmable circuit.

31. The method of claim 30, further comprising operating in the configuration after downloading the configuration data from the memory.

32. A method, comprising:

downloading into a programmable circuit first firmware that represents a first configuration;

operating the programmable circuit in the first configuration;

downloading into the programmable circuit second firmware that represents a second configuration; and

operating the programmable circuit in the second configuration after downloading the second firmware.

33. The method of claim 32 wherein downloading the second firmware comprises:

sending the second firmware to the programmable circuit;

loading the second firmware into a memory with the programmable circuit while the programmable circuit is operating in the first configuration; and

downloading the second firmware from the memory into the programmable circuit.

34. The method of claim 32 wherein downloading the second firmware comprises:

determining whether the second firmware is stored in a memory coupled to the programmable circuit;

sending the second firmware to the programmable circuit only if the second firmware is not stored in the memory;

loading the second firmware into the memory with the programmable circuit while the programmable circuit is operating in the first configuration; and

downloading the second firmware from the memory into the programmable circuit.

35. The method of claim 32 wherein:

operating the programmable circuit in the first configuration comprises testing the programmable circuit; and

downloading the second firmware comprises downloading the second firmware only if the programmable circuit passes the testing.

36. A method, comprising:

downloading first and second firmware into first and second programmable circuits, respectively;

operating the first and second programmable circuits in the first and second configurations, respectively;

downloading third and fourth firmware into the first and second programmable circuits, respectively, via the first programmable circuit; and

operating the first and second programmable circuits in the third configuration and fourth configurations, respectively.

37. The method of claim 36 wherein downloading the first and second firmware comprises downloading the first and second firmware into the first and second programmable circuits, respectively, via a test port.

38. The method of claim 36 wherein:

operating the first and second programmable circuits in the first and second configurations comprises testing the first and second programmable circuits; and

loading the third and fourth firmware into the first and second programmable circuits comprises,

loading the third firmware only if the testing indicates that the first programmable circuit is functioning as desired, and

loading the fourth firmware only if the testing indicates that the second programmable circuit is functioning as desired.